

Characterization of silicon qubit devices fabricated on 300 mm wafers

Master's project starting WS2019/20

Scientific background The electron spin confined in a silicon quantum dot is an ideal platform for the implementation of a long-lived and precisely controlled quantum bit (qubit). Single- and two-qubit manipulation, detection and initialization has been demonstrated for this kind of qubit. MOS-type device fabricated on 300 mm wafers in industrial silicon fabrication lines facilitates higher fabrication throughput and reproducibility, and pave the way to scalable quantum computing.

Research goal We are going to characterize industrially made, electrostatically defined tunnel-coupled double quantum dots (DQDs) formed in a Si-MOS gate architecture at an operation temperature of ~ 10 mK. These devices host up to two spin qubits and have several advantages: Firstly, in silicon, the coupling to nuclear spins and thus the spin decoherence is reduced. Secondly, the possibility of highly developed industrial fabrication techniques improves the reproducibility of electrostatically defined quantum dots. We will evaluate the second argument in cooperation with industrial (imec) and academic partners.

Your task You will learn how to tune Si qubit devices, in order to form single-electron-transistors used as charge detectors and to form quantum dots trapping the qubits. For device tuning, you sweep the voltages of metallic gates patterns (Fig. 1). Simulations of the gate induced electrical potential will support the voltage tuning and let us gain insight on potential noise and disorder in these devices.

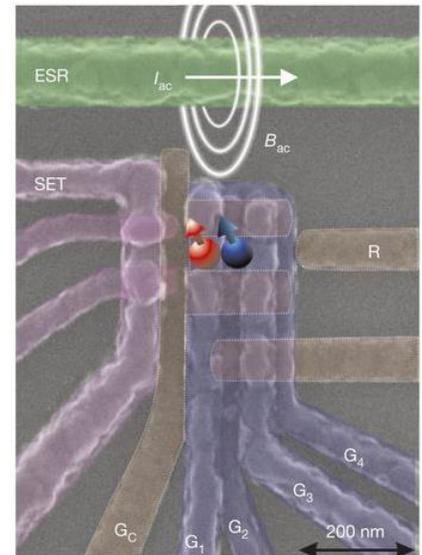
You will gain experience in

- Low temperature transport measurements at 10 mK
- High-frequency, low-noise electrical measurement techniques
- Developing and improving measurement schemes/software
- Data analysis using python and matlab
- Numerical simulations using the COMSOL physics

Furthermore, you will attend group seminars and journal clubs to learn about new developments in quantum computing.

Cooperation partners: Interuniversity Microelectronics Center (IMEC)

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*Scanning electron micro-graph of the metallic gates on top of a double quantum dot silicon sample. The gate pattern consists of several insulated layers. The positions of the trapped electrons are indicated [from M. Velthorst et al., A two-qubit logic gate in silicon., Nature **526**, 410-414 (2015)]*